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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

SRIRAM VAJAPEYAM, ET AL.

Application No.: 10/037,666

Filed: January 3, 2002

For: **DEPENDENCE-CHAIN PROCESSOR**

Art Group: 2819

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to Rule 1.97, Applicant desires to make of record the reference(s) set forth on the attached Form PTO 1449 (or PTO/SB/08). A copy of each reference is submitted herewith.

It is hereby stated that this Information Disclosure Statement is being filed prior to the issuance of the initial office Action, therefore no petition or fee is required. However, in the event a petition is needed for consideration of this Information Disclosure Statement, Applicant hereby so petitions.

Please charge any additional fee due to Deposit Account 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: April 04, 2002

Jonathan S. Miller, Reg. No. 48,534

12400 Wilshire Blvd., 7th Floor
Los Angeles, California 90025
Telephone: (310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 to the Patent and Trademark Office on: *April 04, 2002*

Lillian E. Rodriguez *04/04/02*

Date

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Form PTO-1449 (Modified)	Atty Docket No. 42390P11927	Application No. 10/037,666
List of Patents & Publications Statement	Applicant(s): Sriram Vajapeyam, et al.	
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U.S. PATENT DOCUMENTS

Exam. Initials		Document Number	Date	Name	Class	Sub-class	Filing Date (if appropriate)
	AA	5,699,537	12/16/1997	Sharangpani, et al.			
	AB						
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FOREIGN PATENT DOCUMENTS

Exam. Initials		Document Number	Date	Country	Class	Sub-class	Translation Yes	Translation No
	AL							
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OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

Exam. Initials		Document Identification
	AR	Yuan Chou, John Shen, "Instruction Path Coprocessors", In Proceedings of 27th Annual International Symposium on Computer Architecture, pgs. 270-281, June 2000.
	AS	R. Iannucci, "Toward a Dataflow/von Neumann Hybrid Architecture", In Proceedings of 15th International Symposium on Computer Architecture, pgs. 131-140, 1988.
	AT	S. Palacharla, James Smith, "Complexity-Effective Superscalar Processors", In 24th International Symposium on Computer Architecture, pgs. 206-218, Denver, CO, June 1997.

Examiner: _____ Date Considered: _____

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Exam. Initials		Document Identification
	AR	J.E. Smith, "Instruction-Level Distributed Processing," IEEE Computer, April 2001.
	AS	Sriram Vajapeyam, Tulika Mitra, "Improving Superscalar Instruction Dispatch and Issue by Exploiting Dynamic Code Sequences," 7th International Symposium on Computer Architecture, India, December 1997.
	AT	

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Exam. Initials		Document Identification
	AR	Sanjay J. Patel, Steven S. Lumetta, "rePLay: A Hardware Framework for Dynamic program Optimization." Tech. Rep. CRHC-99-16, Center for Reliable High-Performance Computing, Univ. Illinois, Dec. 1999.
	AS	Narayan Ranganathan, Manoj Franklin, "An Empirical Study of Decentralized ILP Execution Models," In 8th International Conference on Architectural Support for Programming Languages and Operation Systems, pgs. 271-281, October 1998.
	AT	Narayan Ranganathan, Manoj Franklin, "The PEWs Microarchitecture: Reducing Complexity Through Data-Dependence Based Decentralization," Microprocessor and Microprocessing Systems, 1998.

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Exam. Initials		Document Identification
	AR	Eric Rotenberg, Steve Bennett, James E. Smith, "A Trace Cache Microarchitecture and Evaluation", IEEE Transactions on Computers, 48(2): 111-120 (1998).
	AS	Eric Rotenberg, "Trace Processors: Exploiting Hierarchy and Speculation". Ph.D. Thesis, Computer Sciences Dept. Univ. of Wisconsin - Madison (1996).
	AT	

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OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

Exam. Initials		Document Identification
	AR	Sanjay J. Patel, Tony Tung, Satarupa Boe, Matthew M. Crum, "Increasing the Size of Atomic Instruction Blocks Using Control Flow Assertions," Proceedings of 33rd Annual International Symposium on Micro Architecture, 2000.
	AS	Amir Roth, Guri Sohi, "Speculative Data-Driven Sequencing for imperative Programs," UW-Madison TechReport, March 2000.
	AT	J.E. Smith, "Instruction-Level Distributed Processing," Proc. Int'l. Symp. on High-Performance Computing, Dec. 2000.

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